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In The Claims

Claims 56-58, 71, and 72 are pending in the application with claim 56 amended herein, new claims 71 and 72 added herein, and claims 40-55 and 70 canceled herein. Claims 1-39 and 59-69 were previously canceled.

Claims 1-55 (canceled).

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56. (currently amended) Integrated circuitry comprising:

a semiconductive substrate;

an electrically insulative borophosphosilicate glass (BPSG) layer over the semiconductive substrate;

a series of first conductive polysilicon lines directly on and in contact with [[over]] the BPSG layer, the first series conductive lines having individual pairs of respective sidewalls;

electrically insulative oxide material on and in contact with respective first series conductive lines, a top of the insulative oxide material over at least some of the first series conductive lines defining a first plane;

a plurality of insulative oxide sidewall spacer pairs, individual spacer pairs being on respective sidewall pairs of individual first series conductive lines, having respective spacer tops that are coplanar with the first plane, and being connected with the electrically insulative oxide material over the respective individual first series conductive lines;

individual first series conductive lines being effectively insulated by the BPSG layer, the respective sidewall spacer pairs, and the respective insulative oxide material; and

a series of second conductive aluminum-containing lines having respective line tops at least some of which define a second plane that is coplanar with said first plane, the series of second conductive lines being directly on and in contact with [[over]] the BPSG layer and the first series conductive lines providing cross-talk shielding for the second series conductive lines.

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57. (previously presented) The integrated circuitry of claim 56, wherein first series conductive lines have elevational thicknesses in a range from 2000 Angstroms to 10,000 Angstroms.

58. (previously presented) The integrated circuitry of claim 56, wherein individual second series conductive lines have substantially a common lateral cross sectional shape.

Claims 59-70 (canceled).

71. (new) The integrated circuitry of claim 56 wherein the first conductive lines and the second conductive lines are electrically isolated from one another laterally solely by the spacers.

72. (new) The integrated circuitry of claim 56 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.